Cont

one pipeline is controlled by (i) the assignment of one of a plurality of values to at least first, second, and third of said data bits of said at least one branch instruction, said first, second, and third bits adapted to define at least four discrete branch modes; and (ii) the execution of at least one subsequent instruction within said pipeline based on said assigned values of said first, second, and third data bits, when said at least one branch instruction is decoded.

42. The digital processor of Claim 41, wherein first and second of said at least four branch modes implement one- and two-cycle stalls within said pipeline, respectively.

43. The digital processor of Claim 41, wherein at least one of said at least four branch modes comprises a user-configurable mode.

REMARKS

Claims 1-32 were pending in the application. By this paper, Applicant has cancelled Claims 6-13, 21-22, and 24 without prejudice, amended Claims 1, 14, 17, 20, and 23, and added new Claims 33-43. Accordingly, Claims 1-5, 14-20, 23, and 25-43 are presented herein for examination.

Interview

Applicant wishes to thank the Examiner for the courtesy of the personal interview of February 6, 2003.

Amendments to Specification

1. By this paper, Applicant has amended the title of the invention to include the phrase "multi-mode" pursuant to the Examiner's objection in Par. 7, page 3 of the Office Action. Applicant respectfully submits that the title as amended is completely descriptive of the invention as claimed, and that any further "description" or modification of the title would be disconsonant or restrictive with respect to the scope of Applicant's broadest claims. Accordingly, Applicant submits that the objection is overcome.

2. By this paper, Applicant has amended page 11 of the specification to clarify the description of Table 3, pursuant to the Examiner's objection in Par. 8, page 3 of the Office Action. Applicant respectfully submits that the objection is now overcome.

3. By this paper, Applicant has amended page 13 of the specification to include serial numbers and filing dates of the cited applications (also previously listed in the "related Applications" section added via preliminary amendment), pursuant to the Examiner's objection in Par. 9, page 3 of the Office Action. Applicant respectfully submits that the objection is now overcome. Applicant assumes herein that the Examiner's reference to "the abstract of the disclosure" in Par. 9 is a typographical error.

4. By this paper, Applicant has amended Claim 20 in accordance with the Examiner's objections of Pars. 10 and 11 on pages 3-4 of the Office Action. Applicant submits that these objections are now overcome.

5. Per Par. 11, Applicant has cancelled the cited feature(s) from Claim 20 which formed the basis of the drawing rejection. Accordingly, Applicant submits that the drawing corrections referenced in the Par. 12 of the Office Action are now moot.

6. By this paper, Applicant has cancelled Claim 12, thereby rendering the Examiner's objections of Par. 13 of the Office Action moot.

7. By this paper, Applicant has amended Claim 17 ("addition of "at least in part") to correct the defect cited in Par. 14 of the Office Action. Applicant submits that this objection is now overcome.

Rejections Under 35 U.S.C. §§102 and 103

By this paper, Applicant has amended various of the claims as follows to overcome the Examiner's rejections, as discussed in detail below.

Claims 1, 14, 17, and 23 – Independent Claims 1, 14, 17, and 23 as amended now include limitations relating to the recited jump instruction having at least one user-configurable mode associated therewith. Support for this amendment is found, *inter alia*, in Table 1 and page 11, lines 18-19. See also, generally, the discussion of Fig. 4. None of the cited references including U.S. 4,755,966 to Lee ("Lee") seemingly teach or suggest providing at least one user-

configurable mode (e.g., delay slot mode) which can be used for branch/jump control or otherwise. Accordingly, Applicant submits that Lee cannot anticipate, nor can any combination of the cited references render obvious, the inventions of Claims 1, 14, 17 and 23 as amended herein since none teaches or suggests the aforementioned limitation.

Claim 20 – Regarding independent Claim 20, Applicant has herein amended this claim to include limitations relating to defining a plurality of jump delay slot modes comprising; (i) executing a subsequent instruction under all circumstances; (ii) executing a subsequent instruction only if jumping occurs; (iii) stalling the pipeline for one cycle if jumping occurs; and (iv) stalling the pipeline for two or more cycles if jumping occurs. Support for this amendment is found, *inter alia*, at Table 3 of Applicant's specification as filed. None of the cited references appear to teach or suggest provision of such modes. It is significant to note that Lee teaches only three discrete modes associated with the combined single "displacement" and "nullify" bits, respectively; i.e., "01" mode which produces a nullify or execute operation based on branch status; "11" mode which produces an execute or nullify operation based on branch status (inverse of "01" mode); and "00/10" modes which produce execute operations under all branch conditions. See, e.g., Fig. 3 of Lee. Lee teaches or suggests no fourth discrete mode, let alone a fourth mode which allows selection of different number of stall cycles from another mode. Accordingly, Applicant submits that Lee cannot anticipate, nor can any combination of the cited references render obvious, the invention of Claim 20 as amended herein since none teaches or suggests the aforementioned limitations.

Based on the foregoing, Applicant respectfully submits that independent Claims 1, 14, 17, 20, and 23 as amended herein define patentable subject matter, and are in condition for allowance. Furthermore, the dependent claims associated with the foregoing independent Claims are also allowable.

New Claims

By this paper, Applicant has added new independent Claims 33-41, as described below.

New Claim 33 includes limitations relating to at least one user-configurable mode, similar to that previously described with respect to Claims 1, 14, 17, and 23.

Table 2 is a truth table derived from the defined jump delay slot modes of Table 1:

Table 2

	Condition Truth	
Jump Delay Slot Mode	**Jump Taken**	**No Jump Taken**
.nd	One cycle stall or bubble	Delay slot instruction execution
.d	Delay slot instruction execution	Delay slot instruction execution
.jd	Delay slot instruction execution	No delay slot instruction execution

The following assembly language code illustrates examples of the syntax and operation of each of the respective jump delay slot modes of Table 1 using a conditional branch instruction (beq) to program location 'target' followed by a mathematical (add) instruction:

```
(1)   beq.nd target      ;
      add    r1,r1,1     ; "add" not executed if jump taken

(2)   beq.d  target      ;
      add    r1,r1,1     ; "add" always executed

(3)   beq.jd target      :
      add    r1,r1,1     ; "add" executed only if jump taken
```

The fourth mode ("11") of Table 1 may be used for other jump mode or non-jump mode functions as desired, thereby affording the programmer even further flexibility. Additionally, while two bits of the instruction word are illustrated in the embodiment of Table 1, it will be appreciated that other numbers and arrangements of bits (including their position within the instruction word and their syntax) may conceivably be used. For example, three non-contiguous bits could be used to represent up to eight separate jump delay slot modes.

Table 3 illustrates a second embodiment of the jump delay slot modes of the invention utilizing four jump delay slot modes (plus four reserved) based on three data bits within the IW:

New Claims 34 and 36 includes limitations assigning one of a plurality of values to first and second of data bits of at least one jump instruction, the first and second bits adapted to define four discrete jump modes. None of the cited art appears to teach or suggest four discrete jump modes, as previously cited with respect to Claim 20.

New Claim 35 includes similar limitations relating to four discrete jump modes, as well as one of the four modes comprising a user-defined mode.

New Claim 37 defines an extensible pipelined digital processor having an instruction set comprising a plurality of basecase instructions and at least one extension instruction, at least one of said basecase and extension instructions comprising a branch instruction having at least one user-configurable mode and a plurality of other modes controlling the execution of at least one instruction in a delay slot following the branch instruction within said pipeline. Support for this claim is found at, *inter alia*, page 15, line 18, as well as in Applicant's co-owned application incorporated by reference at page 14, lines 1-9 of the present specification as filed. Applicant submits that none of the cited art teaches or suggests use of such branch instruction having multiple modes within an extensible/user-configurable processor architecture as recited.

Similarly, new Claims 38 and 40 recites limitations relating to an extensible pipelined digital processor having a branch instruction including four discrete modes controlling the execution of at least one instruction in a delay slot following the branch instruction.

New Claim 39 recites an extensible pipelined digital processor comprising a basecase processor core configuration including a base instruction set; and at least one user-configured extension instruction comprising a branch instruction having at least one user-defined mode and a plurality of other modes controlling the execution of at least one instruction in a delay slot following the branch instruction.

Lastly, new Claim 41 recites a digital processor having a branch instruction, wherein the execution of instructions within the pipeline is controlled by (i) the assignment of one of a plurality of values to at least first, second, and third data bits of the branch instruction, the first, second, and third bits adapted to define at least four discrete branch modes. None of the cited references teach or suggest use of three bits within a branch/jump instruction for controlling the operation of delay slot(s).

Accordingly, Applicant submits that new Claims 33-43 define patentable subject matter and are in condition for allowance as well.

Applicant hereby specifically reserves the right to prosecute claims of different or broader scope, including those cancelled without prejudice herein, in a continuation or divisional application.

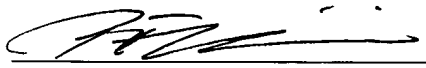
Applicant notes that any amendments, cancellations, or additions made herein are made solely for the purposes of more clearly and particularly describing and claiming the invention, and not for purposes of overcoming art or for reasons relating to patentability unless otherwise stated. The Examiner should infer no (i) adoption of a position with respect to patentability, (ii) change in the Applicant's position with respect to any claim or subject matter of the invention, or (iii) acquiescence in any way to any position taken by the Examiner, based on such amendments, cancellations, or additions.

If the Examiner has any questions or comments which may be resolved over the telephone, he is requested to call the undersigned at (858) 675-1670.

Respectfully submitted,

GAZDZINSKI & ASSOCIATES

Dated: March 17, 2003

By: 

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4. "Kill" signal:

```
ip2killnext<= '1'    WHEN    ((ip2dd = dmk ) AND ip2bch = '1')
                     OR      ((ip2dd = dmnd) AND ip2jumping = '1')
                     OR      ((ip2dd = dmjd) AND ip2nojump = '1')
ELSE
                '0';

p2killnext <= ip2killnext;
```

It is noted that the ip2killnext instruction of the illustrated embodiment includes p2iv (pipeline stage 2 instruction valid signal) and a full decode for a jump operation, so that it can be used within the pipeline control logic ("pipectl") without any further decode apart from en2 (pipeline stage 2 enabled/stalled signal). This feature reduces decode delays and permits faster instruction execution. While the decode technique used in this example results in the foregoing operational benefits, it will be recognized that this technique is not essential to the practice of the present invention.

Appendix A illustrates one exemplary embodiment of the VHDL used for synthesis of the foregoing jump delay slot modes of the present invention.

Appendix B provides an exemplary synthesis script for delay slot synthesis using the Synopsys® synthesis engine.

It is also noted that the methods and apparatus of the present invention may be used in conjunction with (alone or collectively) other methods of pipeline control and interlock including, inter alia, those disclosed in Applicant's co-pending U.S. Patent Application Serial No. 09/523,871 filed March 13, 2000 entitled "Method And Apparatus For Jump Control In A Pipelined Processor," as well as those disclosed in Applicant's co-pending U.S. Patent Application Serial No. 09/524,179 filed March 13, 2000 entitled "Method And Apparatus For Processor Pipeline Segmentation and Reassembly," both filed contemporaneously herewith, both being incorporated by reference herein in their entirety. Furthermore, various register encoding schemes, such as the "loose" register encoding described in Applicant's co-pending U.S. Patent Application Serial No. 09/524,178 filed March 13, 2000 entitled "Method and Apparatus for Loose Register Encoding Within a Pipelined Processor" filed contemporaneously herewith and incorporated by reference in its entirety herein, may be used in conjunction with the jump delay slot invention described herein.